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## **Circuit Design For Cmos Vlsi**

Unit inverter circuit. All

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images adapted from  
CMOS VLSI Design (4th  
ed.) 1 by Neil H.E.

Weste and David  
Money Harris

$\frac{\text{logical effort}}$

$(g) = \frac{\text{effective capa}}$

$\frac{\text{citanace}}{\text{effective capacitance of an inverter}}$

$= \frac{3C}{3C} = 1$

For a 3-input NAND  
gate shown below, the  
capacitor presented at  
the input B is  $(3C + 2C$   
 $= 5C)$ .

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## **Transistor Sizing in VLSI Design Using the Linear Delay ...**

The method of logical effort, a term coined by Ivan Sutherland and Bob Sproull in 1991, is a straightforward technique used to estimate delay in a CMOS circuit. Used properly, it can aid in selection of gates for a given function (including the number of stages necessary)

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and sizing gates to achieve the minimum delay possible for a circuit.

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